P2 concld

ground in response to the logic state 0 signals on terminals 514,516,518, respectively. Referring now to FIG. 33B, on phase P1 of the 3-phase clock (FIG. 32) all of the charging switches S3, S6, S9 and S12 (FIG. 31) and the output switch S204 are in an open condition, and all of the charge sharing switches S200, 201, 202, 203 are in a closed condition, whereby charge is redistributed and resulting in the total charge on all of the capacitors being divided among all of the capacitors. If the capacitors C1, C2, C3, C4 all have the same capacitance value C, then the charge is shared equally so that the voltage across each capacitor becomes $V_{ref}/4$. Referring now to FIG. 33C, on P2 of the 3-phase clock (FIG. 32) switch S200 is in the closed condition because P2 has a logic 1 state and bit_1 has a logic state 1. Switches S201, S202, S203 are in the open condition because bit_2, bit_3, bit_4, have a logic state 0. Output switch S204 is in the closed condition, and capacitor C1 (FIG. 31) of one-bit DAC 162 delivers its charge to the output terminal 510. Consequently, the total charge delivered to the output terminal 510 is equal to C*Vref/4.

Please amend the paragraph beginning on page 32, line 26 to read as follows:

A3

FIGS. 34A-34C are block diagrams showing the operation of the squaring circuit 500 of FIG. 31 for each of the 3 clock phases in the event that input terminals 512, 514, 516, 518 are supplied with digital bit signals bit_1, bit_2, bit_3, bit_4, having logic states of 1, 1, 0, 0, respectively. Tables show the relationship between the clock phase, and the state (i.e., voltage and charge) of the capacitors in the one-bit DACs. Referring now to FIG. 33A, on phase P3 of the 3-phase clock (FIG. 32), all of the charge sharing switches S200, S201, S202, and S203 and the output switch S204, are in the open condition. The capacitor C1 and the capacitor are each charged to V_{ref} in response to the logic state 1 on terminal 512 and 514, respectively. Capacitors C3 and C4 are all discharged to ground in response to the logic 0 signals on terminals 516, 518, respectively. Referring now to FIG. 34B, on phase P1, all of the charging switches S3, S6, S9 and S12 (FIG. 31) and the output switch S204 are in an open condition, and all of the charge sharing switches S200, 201, 202, 203 are in a closed condition, whereby charge is redistributed and resulting in the total charge on all of the capacitors being divided among all of the capacitors. If the capacitors C1, C2, C3, C4 all have the same capacitance value C, then the charge is shared equally so that the voltage across each capacitor becomes $V_{ref}/2$. Referring now to FIG. 33C, on phase P2 of the 3-phase clock (FIG. 32), switch S200 is in the closed condition because P2 has a logic state 1 and bit_1 has a logic state 1. Switch S201 is in the closed condition